Active Gate Control Methods for the Turn-On of High-Voltage Power MOSFETs in Hard Switching Applications

Stephan Brueske, Friedrich W. Fuchs
Institute for Power Electronics and Electrical Drives
Christian-Albrechts-University of Kiel
Kaiserstr. 2, 24143 Kiel, Germany
Email: sbr@tf.uni-kiel.de, fwf@tf.uni-kiel.de

Abstract
An analysis of turn-on active gate control for high-voltage power MOSFETs to reduce the reverse-recovery current of the body diode is presented. The turn-on switching behaviour of the MOSFETs is analysed in theory and simulation when controlled by two dedicated gate drive circuits. The performance depending on the dedicated gate drive circuits is investigated and compared with that of the common basic gate drive circuit. One gate drive circuit is investigated practically.

1 Introduction
Power semiconductors play a significant role in designing of AC-DC converters or DC-DC converters. In some regenerative and automotive applications high-voltage power MOSFETs (Superjunction MOSFET, SJ MOSFET) are an interesting alternative for the commonly used IGBTs. Especially in multilevel converter topologies applied to low power where the blocking voltage is smaller, SJ MOSFETs are favourable. The advantages of SJ MOSFETs compared with IGBTs are the lower power losses in partial load operation and the better switching performance.

The disadvantage of the superjunction technology is the high loss during full load operation due to the on-state voltage drop which is dependent on $R_{\text{DS, on}}$. A comparison of SJ MOSFETs and IGBT revealed that the use of SJ MOSFETs in an electric vehicle is reasonable if the blocking voltage is smaller than 200 V [1]. In order to improve the switching performance active gate control methods can be used. Active gate control methods are already investigated for IGBTs [2] and low-voltage power MOSFETs [3] and in those applications the switching losses can be reduced or the switching performance improved. Here active gate control methods for high voltage power MOSFETs are investigated under hard switching conditions.

In a first step the switching behaviour of high-voltage power MOSFETs is presented. In contrast to low-voltage power MOSFETs, the turn-on losses are dominating. One problem related to high-voltage power MOSFETs is the high reverse-recovery effect of the internal body diode [4]. The solution could be to use a SiC- or a Si-Diode in parallel to the internal body diode of the MOSFET [5] and in case of a Si-Diode a second additional diode in series with the MOSFET. This is necessary to prevent the reverse-recovery current through the internal body diode. This solution means lower efficiency and higher costs. Another possibility is to influence the switching behaviour of the MOSFET by active gate control to reduce the reverse-recovery current which will be investigated in this paper.

This paper is structured as follows: In section 2 the turn-on switching behaviour of the SJ MOSFET is analysed and approaches to modify the current slope are described. Then in section 3 the two two-level gate voltage control methods are described and compared. In section 4 simulation results are presented and in section 5 laboratory results are presented and analysed. Finally in chapter 6 a conclusion is drawn and prospects for further research are given.

2 Turn-on Switching Behaviour Analysis
In general the switching behaviour of the high-voltage SJ MOSFET is similar to the switching characteristic of a low voltage power MOSFET. For the analysis the test circuit for the double pulse test, presented in figure 1a, is used where the SJ MOSFET M2 is investigated and M1 is used as a diode. For both SJ MOSFETs the internal structure and stray inductances of the connections are given. The test circuit represents the common configuration of a hard switching converter leg. This paper is focused on the
The turn-on behaviour of the SJ MOSFET because the reverse-recovery current of the internal body has to be considered in hard-switching topologies.

Figure 1b shows the general turn-on waveform characteristic of a MOSFET [6] which are applicable for the SJ MOSFET. $V_{th}$ is the threshold voltage of the SJ MOSFET and $V_{miller}$ is the voltage level of the miller plateau. During the turn-on process the SJ MOSFET is working in the saturation region [6]. In the time interval $T_{2,4}$ the current $i_d$ is greater than 0 A and has not reached its final value $I_{DD}$. The current slope of $i_d$ in $T_{2,4}$ can be analysed for $t < t_3$ (equation 1) and $t > t_3$ (equation 2) separately [6]. $S$ is the snappiness factor of the internal body diode which describes the turn-off behaviour of a diode.

$$\frac{di_d}{dt} \sim \frac{1}{L_{s,\text{int}} + L_{s,\text{ext}}} \cdot \left(V_{GG} - v_{gs}(t) - (R_{G,\text{int}} + R_{G,\text{ext}}) \cdot i_g(t) - L_{GS} \cdot \frac{di_g}{dt}\right)$$  \hspace{1cm} (1)

$$\frac{di_d}{dt} \sim -\frac{1}{S} \left| \frac{di_d}{dt} \right|_{i_d=I_{DD}}$$  \hspace{1cm} (2)

The proportionality of the peak current $i_{d,\text{peak}}$ is given in equation 3. Therefore $i_{\text{peak}}$ can be reduced by increasing the gate resistance $R_{G,\text{ext}}$ or the stray inductance ($L_{s,\text{int}}, L_{s,\text{ext}}, L_{GS}$) or by decreasing $V_{GG}$. Another possibility is the injection of an additional gate current $i_g(t)$.

$$i_{d,\text{peak}} \sim \sqrt{\frac{di_d}{dt}}_{i_d=I_{DD}}$$  \hspace{1cm} (3)

Figure 1: Test circuit and general turn-on performance (a) Test circuit for the double pulse test, $M_1$ used as diode, $M_2$ is the device under test (b) Turn-on switching performance of the SJ MOSFET with $R_G = R_{G,\text{ext}} + R_{G,\text{int}}$ [6]

The drain source voltage rise $dV_{ds}/dt$ in time interval $t_3$ to $t_4$ is described by equation 4 [6] with the miller voltage $V_{miller}$ given in equation 5 with $g_{MOSFET}$ as transconductance of the SJ MOSFET. Consequently for a reduction of the switching time $v_{gg}$ should be at its maximum value during time interval $t_3$ to $t_4$.

$$\frac{dV_{ds}}{dt} = -\frac{V_{gg} - V_{miller}}{(R_{G,\text{ext}} + R_{G,\text{int}}) \cdot C_{gs}}$$  \hspace{1cm} (4)

$$V_{miller} = I_{DD} \cdot \frac{1}{g_{MOSFET}} + V_{th}$$  \hspace{1cm} (5)
The common and easiest way of influencing the current slope is the variation of the gate resistor $R_{G,ext}$. The major disadvantage of this solution are the increasing switching losses during turn-on and turn-off. Another possibility is the variation of the applied gate voltage $v_{gg}$ which will be investigated in the following section.

3 Variation of the Gate Voltage

The gate voltage $V_{GG}$ can be adapted in two different ways in order to influence the switching behaviour of the SJ MOSFET during time interval $t_I$ in figure 1b. The idea is to use for a short time a reduced gate voltage during the turn-on process of the SJ MOSFET. Two variants are proposed. Figure 2a illustrates method 1 [2] and figure 2b method 2 [7]. The difference of the two methods is the positioning of the reduced voltage $v_{gg}$ interval.

Method 1 is characterized by a stepwise increase of $v_{gg}$. The reduced voltage level $V_1$ and its time length $T_1$ are the two tuneable parameters. $V_1$ can be selected according to equation 6.

$$\text{minimum} \left( V_{th}, v_{gs,\text{min}}(i_d) \right) < V_1 \leq V_{GG}$$  \hspace{1cm} (6)

The lower boundary $V_{th}$ (threshold voltage) is the lowest possible value of $V_1$ at a small load current $i_d$. The lower voltage boundary rises with an increasing current $i_d$ due to the tranconductance of the SJ MOSFET which is determined by equation 7. This implicates that the selection of the voltage level $V_1$ is dependent of the maximum load current $I_{DD}$.

$$i_{d,\text{max}}(v_{gs}) = g_{\text{MOSFET}} \cdot \left( v_{gs}(t) - V_{th} \right)$$  \hspace{1cm} (7)

Consequently the optimum time value to minimize switching losses is $T_1 = t_3 - t_1$. Method 2 has three tuneable parameters ($T_{2a}$, $T_{2b}$, $V_2$) which can be used to optimize the switching behaviour and is therefore an enhancement of method 1. The difference in comparison to method 1 is the time interval $T_{2a}$ which is used to charge the gate capacity $C_{gs}$ fast. The time interval $T_{2a}$ should end before $i_d$ reaches the load current level $I_{DD}$. $T_{2b}$ has to be selected as $T_{2b} > t_3 - t_1 - T_{2a}$. The whole switching time of method 1 is longer than the switching time of method 2. Therefore the switching losses will be higher in method 1 in comparison with method 2. The disadvantage of method 2 in comparison with method 1 is the more complex gate drive circuit because three tuneable parameters have to be realised.

For both methods the selection of the tuneable time parameters $T_1$, $T_{2a}$ and $T_{2b}$ is dependent on the load current $I_{ld}$. Therefore the realisation of an active gate control circuit by means of a turn-on feedback-control as presented in [2] is possible. In section 4 and 5 the variation of the tuneable parameters and the influence of the load current is investigated.

4 Simulation Results

The performance of SJ MOSFETs with the dedicated active gate control circuits is analysed by simulation. The simulations are implemented in LTSPICE and for the SJ MOSFETs the models offered
by Infineon are used. For the simulative investigation the Infineon SJ MOSFETS IPx65R190CFD (V_{ds,max} = 650 V, I_{DD,max} = 17 A) and IPx65R190E6 (V_{ds,max} = 700 V, I_{DD,max} = 20.2 A) are used. The IPx65R190CFD is very similar to the practically investigated IPx65R190CFDA so that the Infineon transistor model could be used for the simulative investigation. The diode of the IPx65R190CFD has a smaller reverse-recovery charge and therefore a snappier diode behaviour. The double pulse test circuit according to figure 1a is realised with leakage inductances chosen to L_{s,ext} = 10 nH, L_{d,ext} = 5 nH, L_{setup} = 60 nH and L_{GS} = 30 nH. These leakage inductances were adapted according to the laboratory setup. In figure 3a and 3b the turn-on behaviour for both SJ MOSFETs is simulated with different external gate resistances R_{G,ext}. At t = 0 s the turn-on process starts by applying a gate voltage V_{gg} > 0 V. The d\(i_g/dt\) in time interval (t_2 to t_3) is decreasing with an increasing value of R_{G,ext}. The peak current i_{d,peak} and the current slope in time interval (t_3 to t_4) are only slightly decreasing with an increasing R_{G,ext}.

Figure 3: Simulated turn-on performance for different R_{G,ext}: V_{DD} = 400 V, I_{DD} = 11 A, V_{gg} = 14.2 V (a) IPx65R190CFD, (b) IPx65R190E6

4.1 Analysis of method 1

The performance for the variation of the parameter V_1 is depicted in figure 4a and 4b. A higher voltage V_1 extends the turn-on time and is decreasing the d\(i_g/dt\) in time interval (t_2 to t_3) as well as in (t_3 to t_4) and the value of i_{d,peak}. The variation of the parameter T_1 is depicted in figure 5a and 5b. If T_1 is chosen too small, the d\(i_g/dt\) will increase for a short time during current rise time as well as current fall time. Another conclusion which can be drawn is that an increased time interval T_1 does not effect the peak current but
will increase the switching losses a bit because the time interval (t₄ to t₅) is longer where the voltage is \(v_{ds} = V_{miller} - V_{th} > V_{ds,\text{on}}\). In figures 6a and 6b the performance at varied load currents \(I_d\) at constant parameters \(V_1\) and \(T_1\) is investigated. The current slope is nearly constant for the IPx65R190CFD and decreasing over time for the IPx65R190E6. Consequently the relation of \(i_{d,\text{peak}}/I_d\) is constant for the IPx65R190CFD and decreasing for the IPx65R190E6 with higher load currents.

Figure 5: Simulated turn-on performance for method 1 for different \(T_1\): \(V_{DD} = 400\, V\), \(I_{DD} = 11\, A\), \(R_{G,\text{ext}} = 15\, \Omega\), \(V_1 = 8\, V\) (a) IPx65R190CFD, (b) IPx65R190E6

Figure 6: Simulated turn-on performance for method 1 for different \(I_{DD}\): \(V_{DD} = 400\, V\), \(R_{G,\text{ext}} = 15\, \Omega\), \(V_1 = 8\, V\) (a) IPx65R190CFD \(T_1 = 230\, \text{ns}\), (b) IPx65R190E6 \(T_1 = 360\, \text{ns}\)

4.2 Analysis of method 2

The conclusion of the previous chapter for \(T_1\) can be applied for the parameter \(V_{2b}\). The higher gate voltage level can be applied after \(i_d\) reaches its peak value. The simulative results for different voltages \(V_2\) are shown in figure 7a and figure 7b. Comparing those results with figures 4a and 4b it can be noticed that \(i_{d,\text{peak}}\) is identical in case of \(V_1 = V_2\). Thus the turn-on switching time and therefore the turn-on losses can be reduced by using method 2 in comparison to method 1 in case the tuneable parameters are chosen accordingly. In figures 8a and 8b the variation of the parameter \(T_{2a}\) is depicted. In case \(T_{2a} = 10\, \text{ns}\) there is no effect of the parameter on the \(di_{d}/dt\) and \(dv_{ds}/dt\) because \(V_{th}\) is not reached before \(v_{gg}\) is reduced. The comparison of the switching time of method 2 (\(T_{2a} = 10\, \text{ns}\)) and method 1 for the same working point shows that the switching time is shorter for method 2 due to the faster charging of \(C_{gs}\). In figure 9a and 9b the three tuneable parameters are assumed fix and this configuration is tested for different load currents \(I_d\).

In order to reduce losses in a hard-switching converter topology the IPx65R190CFD is preferable in comparison to the IPx65R190E6 because the switching time, the peak current and the turn-on losses are smaller. Therefore in section 5 the IPx65R190CFDA is analysed experimentally.
5 Experimental Results

To verify method 1 experimentally, a turn-on gate driver for the SJ MOSFET is designed according to the block diagramm of figure 10a. The diode is used to prevent an influence of the proposed circuit on the turn-off behaviour of the SJ MOSFET. The two-step gate voltage turn-on waveform $v_{gg}$ without a transistor is shown in figure 10b. For practical application of the proposed method an analysis of the increased switching time and the reduced turn-on gate voltage on the SJ MOSFET is necessary.

In figure 11a the IPW65R190CFDA is tested with varying $R_{G,ext}$. Figure 11b shows the performance for the variation of $V_1$, figure 12a the variation of $T_1$. For the IPW65R190CFDA a satisfying accordance between the simulation results and the experimental results could be obtained regarding the turn-on waveforms. It could be seen that the current slope is reduced with smaller values for $V_1$. From figure 12a it can be concluded that $T_1$ has to be selected accordingly: if $T_1$ is chosen too small, the current
slope and the peak current will increase. This could be avoided by designing $T_1$ larger. As derived in section 3, a time $T_1$ larger than necessary is delaying the switching time. For method 1 it could be concluded that an adaption of $T_1$ to the current working point is recommendable. $V_1$ has to be designed according to the preferred turn-on switching behaviour. In figure 11b the turn-on switching waveforms for constant values of $T_1$ and $V_1$ at different load currents are shown. It could be seen that the parameter $T_1$ could be selected once and that no adaption to the current working point is necessary.

The higher current slope at the beginning of the turn-on process is due to parasitic effects of $L_{GS}$ and the switching characteristic of $v_{gg}$ which is depicted in figure 10b. In table 1 the turn-on losses and the turn-on switching time for different methods is listed. It could be seen that turn-on losses are increasing significantly for method 1 in comparison to the standard gate driver concept.
Method switching time (t1 to t4) in μs Energy losses in (t1 to t4) in mJ
\[ R_{G,ext} = 10 \Omega \] 0.112 0.461
\[ R_{G,ext} = 51 \Omega \] 0.152 0.499
Method 1, \( V_1 = 10 \text{ V}, T_1 = 420 \text{ ns} \) 0.188 0.624
Method 1, \( V_1 = 9.2 \text{ V}, T_1 = 420 \text{ ns} \) 0.208 0.673
Method 1, \( V_1 = 8.2 \text{ V}, T_1 = 420 \text{ ns} \) 0.256 0.807
Method 1, \( V_1 = 7.2 \text{ V}, T_1 = 420 \text{ ns} \) 0.356 1.1
Method 1, \( V_1 = 7.0 \text{ V}, T_1 = 420 \text{ ns} \) 0.428 1.4

Table 1: Comparison of switching time and losses for method 1 and the variation of \( R_{G,ext} \)

6 Conclusion

The turn-on switching behaviour of a SJ MOSFET has been analysed applying two two-level gate voltage steps control methods to influence the turn-on switching behaviour. The methods have been described analytically. Both proposed methods were implemented in LTSPICE and investigated for two different SJ MOSFETs. The first method has a simpler gate drive circuit but has also an inferior turn-on switching performance in comparison with the second proposed gate drive circuit. In the experimental part method 1 has been implemented and tested successfully for one SJ MOSFETs. It has been shown that the peak current and the current slope could be reduced whereas in general the turn-on switching time and therefore turn-on losses increase. Future research could focus on the practically implementation and analysis of method 2. Another possibility is the realisation of a feedback-loop which would adapt the switching behaviour to the current working point. Additionally the voltage level for method 2 during time interval \( T_{2a} \) could be increased to a value greater than \( V_{GG} \).

7 Acknowledgement

The work has been funded by the Interreg IVa - Project as a working package of the eMOTION project.

References